

Proteus

Extensible RISC-V processor & Security Applications





BINSEC













PhD student doing program/protocol verification

* List probably non-exhaustive * Special congrats if you recognize all tools!

BINSEC













PhD student getting paper accepted

* List probably non-exhaustive * Special congrats if you recognize all tools!



* List probably non-exhaustive * Special co

* Special congrats if you recognize all attacks!

DONT WORRY. WE GOT YOUR BAGK



Proteus: An Extensible RISC-V Core for Hardware Extensions

Marton Bognar¹^{*}, Job Noorman¹, Frank Piessens¹





- Static / Dynamic pipeline (textbook implem)
- Optimizations: OoO Speculative Execution, Cache, ~Prefetchers, more to come!
- Configurable: #Exec units, ROB size
- **Extensible**: plugin system
- **SpinalHDL** > Verilog > FPGA / Simulator
- Validate: HW fuzzing / verif. setup (in progress)

PROSPECT: Provably Secure Speculation for the Constant-Time Policy

Lesly-Ann Daniel¹, Marton Bognar¹, Job Noorman¹, Sébastien Bardin², Tamara Rezk³ and Frank Piessens¹

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- HW-SW co-design (SW marks secrets)
- CT code secure against Spectre
- Without sacrificing speculation
- Holds for many variants of Spectre

Wave your troubles awaaaaaay!



Spectre waved away

Architectural Mimicry: Innovative Instructions to Efficiently Address Control-Flow Leakage in Data-Oblivious Programs

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High-speed surfing on the Proteus wave

- HW-SW co-design (new ISA)
- Secure secret-dependent control-flow
- Support for linearization/balancing
- Accelerate CT code

Surf on the wave for extra speeeed!

What comes next?

Better support

- **Compiler** support for HW defenses
- Hardware validation

More features

- Wave away more troubles! (DDP)
- **Surf** faster! (Accelerate CT code)
- Deliver coffee? (But hard problem)







https://github.com/proteus-core

Surf / wave your troubles away with Proteus too!