KU LEUVEN

ProSpeCT: Provably Secure Speculation for the Constant-Time Policy

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SPLiTS Security Workshop

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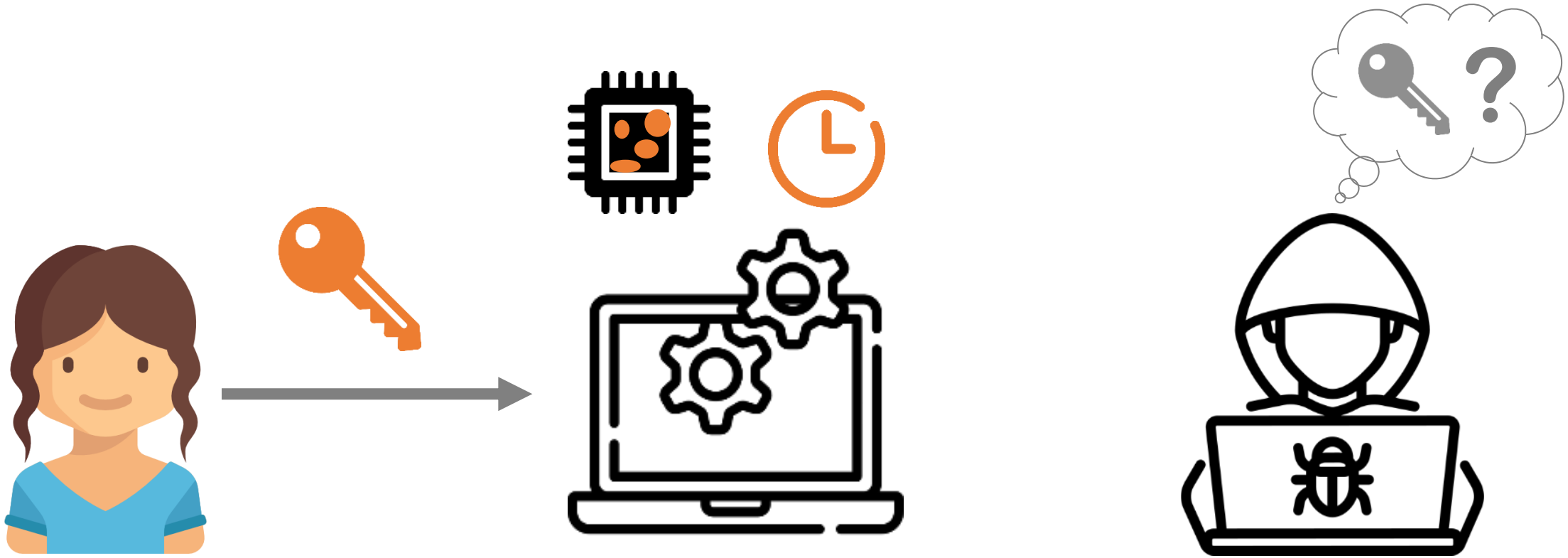
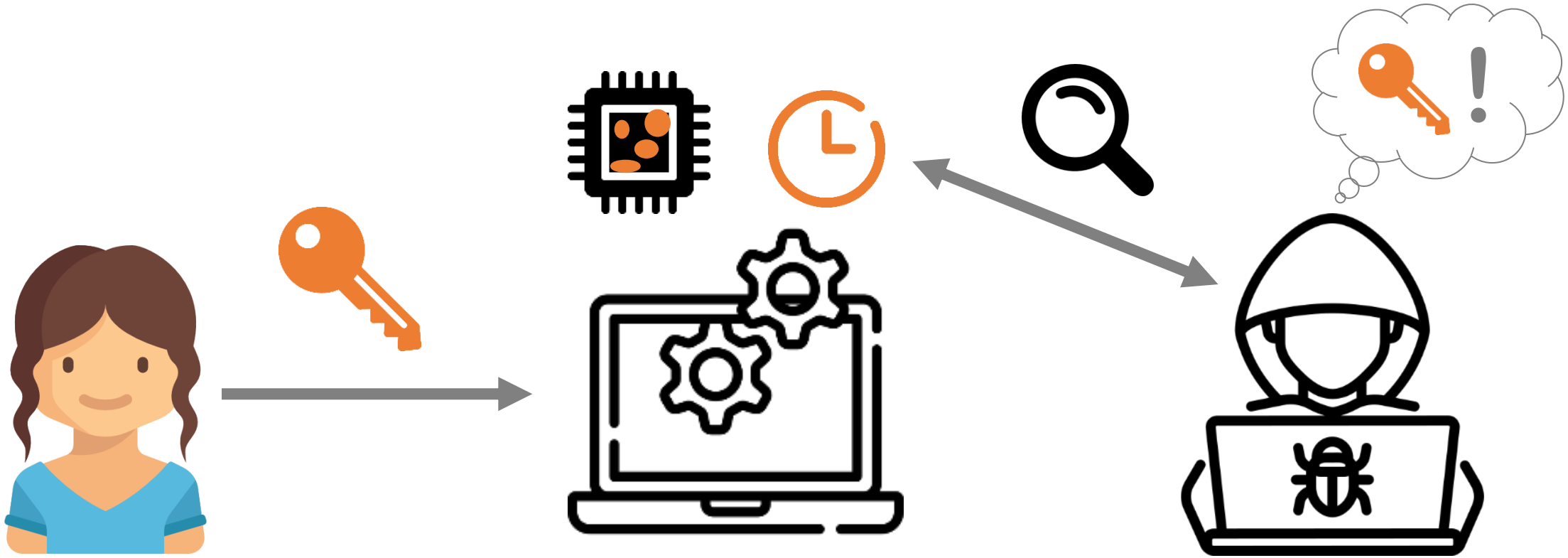
Need to protect against microarchitectural attacks

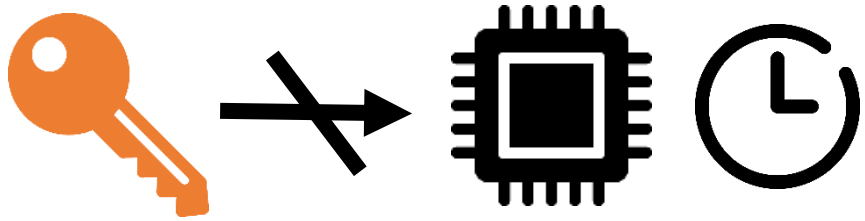


Need to protect against microarchitectural attacks



Easy: constant-time programming!

```
    char array[len]
    char mysecret
1:  if (idx < len)
2:      x = array[idx]
3:      leak(x)
```



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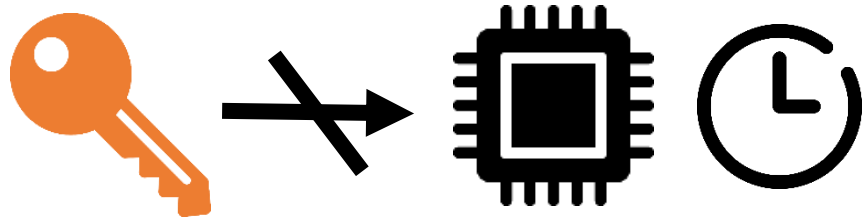

`mysecret` ⇝ `leak()`

De facto standard for crypto

… still vulnerable to Spectre attacks

```
   char array[len]
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1: if (idx < len)
2:     x = array[idx]
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```
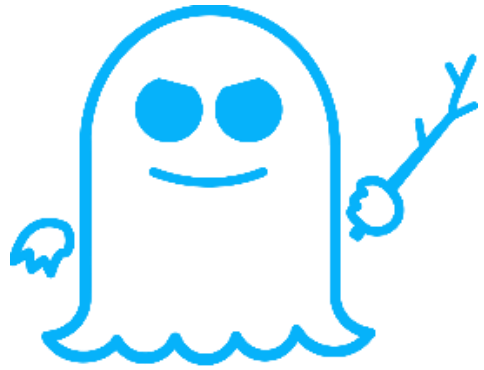

Predict branch taken



… still vulnerable to Spectre attacks

```
   char array[len]
   char mysecret
1: if (idx < len)
2:     x = array[idx]
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```
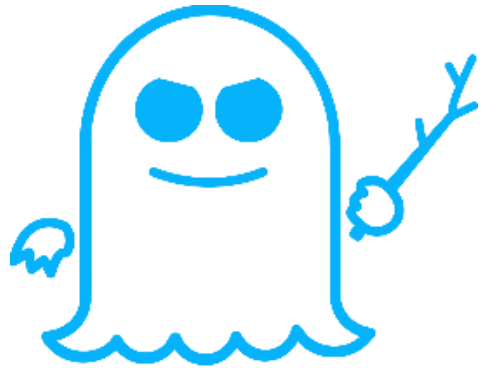

Predict branch taken

`x = mysecret`

Leaks `mysecret` to microarchitecture!



How can I protect my code?

Constant-Time Foundations for the New Spectre Era

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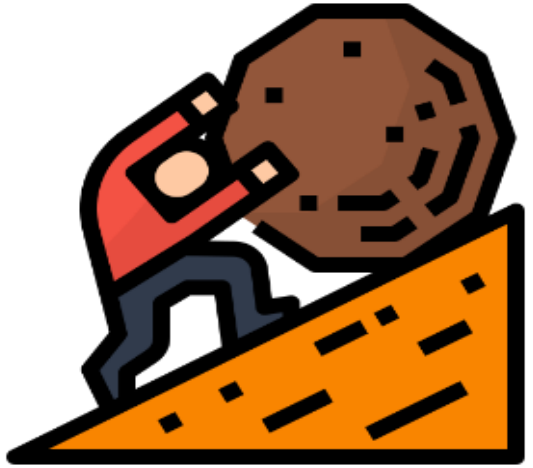
Speculative constant-time

- Hard to reason about
- New speculation mechanisms?



We need Secure Speculation for Constant-Time!

Developers should not care about speculations

Hardware shall not speculatively leak secrets

But still be efficient and enable speculation

Hardware defense:
Secure speculation for constant-time!

Hardware Secrecy Tracking

Software side

- Label secrets
- Constant-time program

Hardware side

- Track security labels
- Secrets do not speculatively flow to insecure instructions

ConTExT: A Generic Approach for Mitigating Spectre

Michael Schwarz[1], Moritz Lipp[1], Claudio Canella[1], Robert Schilling[1,2], Florian Kargl[1], Daniel Gruss[1]
[1]Graz University of Technology [2]Know Center GmbH

SpectreGuard: An Efficient Data-centric Defense Mechanism against Spectre Attacks

Jacob Fustos — University of Kansas
Farzad Farshchi — University of Kansas
Heechul Yun — University of Kansas

Speculative Privacy Tracking (SPT): Leaking Information From Speculative Execution Without Compromising Privacy

Rutvik Choudhary — UIUC, USA
Jiyong Yu — UIUC, USA
Christopher W. Fletcher — UIUC, USA
Adam Morrison — Tel Aviv University, Israel

Illustration with Spectre-v1

```
    char array[len]
    char mysecret
1:  if (idx < len)
2:      x = array[idx]
3:      leak(x)
```

Consider `idx = len`

Illustration with Spectre-v1

```
   char array[len]
   secret char mysecret
1: if (idx < len)
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```

Developer marks secrets

Consider `idx = len`

Illustration with Spectre-v1

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   char array[len]
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Speculative execution

Consider `idx = len`

Illustration with Spectre-v1

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   char array[len]
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Developer marks secrets

Speculative execution

`x = mysecret:secret`

Consider `idx = len`

Illustration with Spectre-v1

```
   char array[len]
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1: if (idx < len)
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```

Developer marks secrets

Speculative execution

`x = mysecret:secret`

Speculative execution + **secret**
=
`x` *not* forwarded to `leak`

Consider `idx = len`

How do I know that my defense works?

How do I know that my defense works?

Challenges

Adapt HW/SW contract framework to account for

- All existing speculation mechanisms (Spectre, LVI)
- Futuristic speculation mechanisms (value prediction)
- Declassification

Our contributions

- ProSpeCT: Formal processor model with HST
  - Proof: constant-time programs do not leak secrets
  - Allows for declassification
  - Generic: all Spectre variants / LVI

- First to consider (Load) Value Speculation
  - Novel insight: sometimes need to rollback *correct* speculations for security

- Implementation in a RISC-V microarchitecture
  - First synthesizable implementation
  - Evaluation: hardware cost, performance, annotations

ProSpeCT: Generic formal processor model for HST

Semantics of out-of-order speculative processor with HST

→ Abstract microarchitectural context

→ Functions $update, predict, next$

Attacker observations/influence

All public values are leaked / influence predictions

Generic/Powerful predictors

Declassify = write secrets to public memory

→ Beware unintentional declassification

ProSpeCT: Generic formal processor model for HST

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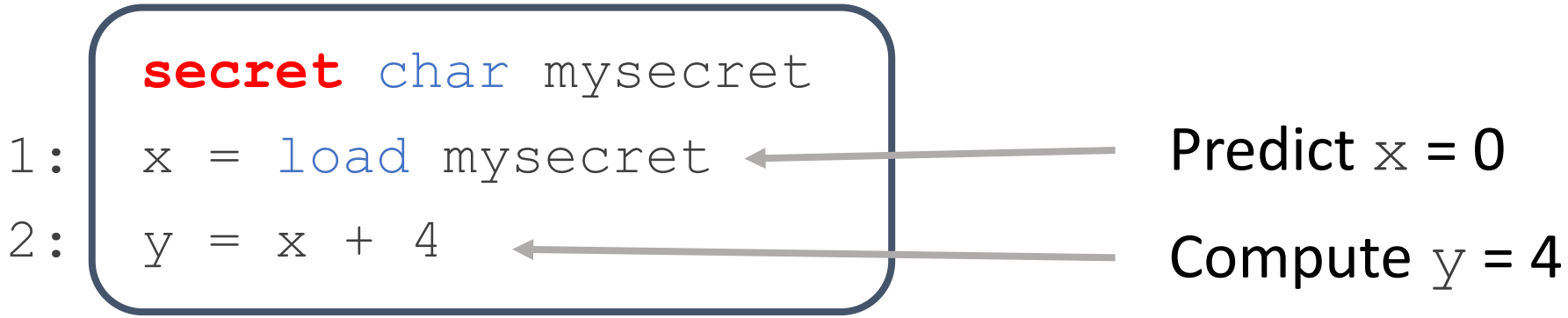
Security proof

Constant-time programs (ISA semantics)
do not leak secrets (micro-arch. semantics)

Load Prediction: Rollback correct executions?

```
   secret char mysecret
1: x = load mysecret
2: y = x + 4
```

Load Prediction: Rollback correct executions?



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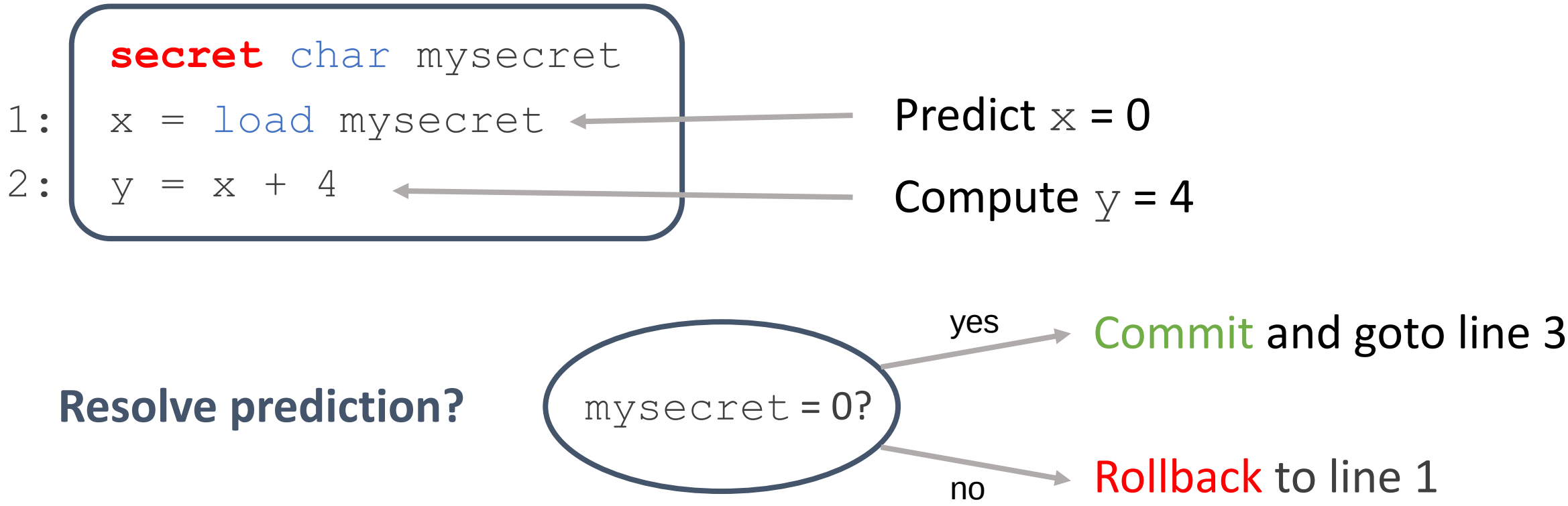
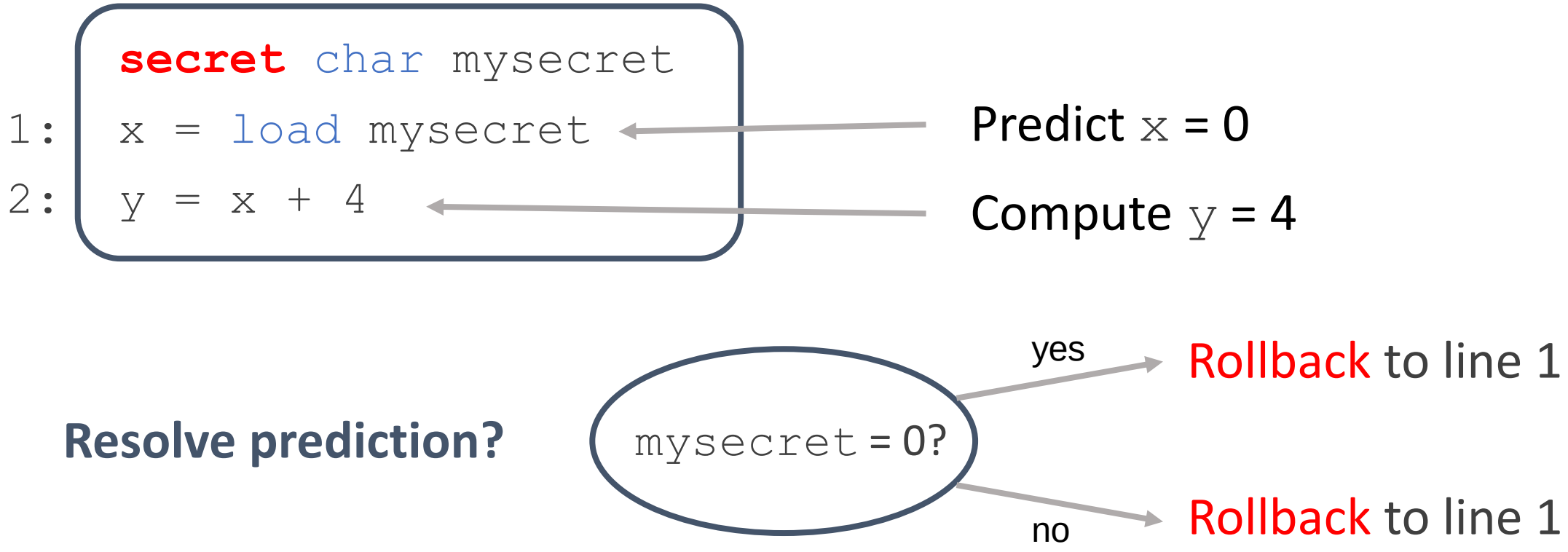


Implicit resolution-based channel!

Load Prediction: Rollback correct executions?



Solution: always rollback when value is secret

Implementation

Prototype RISC-V implementation

On top of Proteus modular RISC-V processor

- Branch target prediction
- Conservative approach
- 2 secret regions defined by CSRs

Limited Hardware Cost

- LUTs: +17%
- Registers: +6%
- Critical path: +2%

Evaluation

4 primitives (HACL*)

- Annotate secret
- Ensure no secrets spilled
- Stack public in 3/4 cases
- ≤1h / primitive

Performance overhead (benchmark from [1])

Speculation/Crypto	25/75	50/50	75/25	90/10
Precise (Key)	**0%**	**0%**	**0%**	**0%**
Conservative (All)	10%	25%	36%	45%

No overhead in software for constant-time code when secrets are precisely annotated

[1] Jacob Fustos, Farzad Farshchi, and Heechul Yun. “SpectreGuard: An Efficient Data-Centric Defense Mechanism against Spectre Attacks”. In: DAC. 2019

Conclusion

Software informs hardware about secrets

Strong security guarantees

End-to-end security for constant-time programs

Low overhead

No software overhead for constant-time code

github.com/proteus-core/prospect

Icons made by **Freepik**, **Vectors Market, monkik** from www.flaticon.com

A step back

RISC-V open standard ISA

→ HW-SW co-design for security

- Proteus: extensible RISC-V processor
- Security extensions
  - ProSpeCT
  - ISA extension for CF balancing/linearization
  - CHERI
  - …

Future work

How to ease adoption of HW-SW co-designs?
→ Need infrastructure around HW-SW contracts

- Secure compilation/compiler support (LLVM, Jasmin?)
- Binary analysis (Binsec/angr)
- Validate HW implementation (fuzzing, verification)

⟹ Márton Bognár

Other relevant projects at KU LEUVEN DistriNet

- Attacks/Defenses for TEEs ⟹ Jo Van Bulck
- Formalization/verification of ISA security guarantees ⟹ Dominique Devriese